

In the claims:

For the Examiner's convenience all pending claims are presented herein. Claims that are unchanged are identified as "unchanged":

1 1. (Amended) A [system to test a bus, the] system comprising:
2 [at least one] instruction memory to store a plurality of predefined bus
3 stimuli [instruction] instructions, the predefined bus stimuli
4 [instruction] instructions representing a plurality of bus
5 [transaction] transactions; and
6 [at least one] one or more phase [generator] generators coupled between
7 [the] a bus and the instruction memory, the [at least] one or more
8 phase [generator] generators to [provide] drive signals [to] on the
9 bus corresponding to [the bus transaction in response to] the
10 predefined bus stimuli [instruction] instructions.

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1 3. (Amended) The system of claim 1, wherein the [instruction comprises an]
2 instructions comprise instruction [word] words having a predefined length.

1 4. (Amended) The system of claim 1, wherein the [at least one phase generator is]
2 one or more phase generators are further responsive to signals received
3 from the bus.

1 5. (Amended) The system of claim [2] 1, further comprising a response memory
2 coupled to the phase generator storing predefined responses to signals
3 received from the bus.

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1 6. (Amended) The system of claim 1, wherein the at least one of the one or
2 more phase [generator] generators includes at least one digital logic device
3 responsive to the instructions and at least one phase engine for controlling
4 timing of the bus stimuli.

1 7. (Unchanged) The system of claim 6, wherein the digital logic device
2 comprises a field programmable gate array.

1 8. (Unchanged) The system of claim 6, wherein the digital logic device
2 comprises an application specific integrated circuit.

1 9. (Unchanged) The system of claim 6, wherein the at least one digital logic
2 device includes a control portion for providing bus control signals and a
3 data portion for sending data to the bus.

1 10. (Unchanged) The system of claim 9, wherein the control portion includes
2 a flow logic device, a request logic device, and a data logic device.

1 11. (Unchanged) The system of claim 6, wherein the at least one phase engine
2 includes at least one logic level translation device.

1 12. (Unchanged) The system of claim 6, wherein the at least one phase engine
2 comprises a system phase engine, an arbitration phase engine, a request
3 phase engine, a snoop/error phase engine, and a data phase engine.

1 13. (Unchanged) The system of claim 9, further comprising a data memory
2 coupled to the data portion.

1 14. (Unchanged) The system of claim 9, wherein the data portion further
2 receives data from the bus.

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15. (Amended) A [system to test a bus, the] system comprising:
an instruction memory for storing [digital data representing] a predefined
sequence of bus stimuli representing a plurality of bus transactions;
a flow logic device responsive to the instruction memory;
a request logic device responsive to the instruction memory;
a data logic device responsive to the instruction memory;
a data memory coupled to the data logic device for storing data to be
exchanged with agents on [the] a bus;
a system protocol generator coupled to the bus and the flow logic device;
an arbitration protocol generator coupled to the flow logic device and the
bus;
a request protocol generator coupled to the flow logic device, the request
logic device and the bus;
a snoop/error protocol generator coupled to the request logic device and
the bus;
a data protocol engine coupled to the data logic device; and
a transaction response memory coupled to the flow logic device and the
request logic device storing digital data representing predefined
responses to signals received from the bus.

16. (Amended) A system [to test a bus, the system] comprising:
a first means for storing instructions representing a plurality of predefined
bus transactions [stimuli]; and
second means for [providing] driving the plurality of predefined bus
transactions as signals [to] on the bus [in response to the stored
instructions].

1 17. (Unchanged) The system of claim 16, further comprising third means for
2 storing data representing predefined responses to signals received from the
3 bus, and wherein the second means implements the predefined responses
4 based on the signals received from the bus.

1 18. (Unchanged) The system of claim 16, further comprising fourth means for
2 controlling the timing of the signals provided to the bus by the second
3 means.

1 19. (Unchanged) The system of claim 16, further comprising fifth means for
2 storing data to be exchanged with agents on the bus, wherein the second
3 means transmits data from the fifth means in response to the instructions
4 stored in the first means.

1 20. (Unchanged) The system of claim 19, wherein the second means further
2 receives data from the bus and stores the data in the fifth means.

1 21. A method for testing a bus comprising:
2 receiving instruction words [representing] corresponding to predefined bus
3 stimuli, the predefined bus stimuli representing a plurality of bus
4 transactions; and
5 executing the plurality of bus transactions by converting the instruction
6 words to signals and driving the signals on the bus [that, when
7 applied to the bus, execute at least one phase of a bus transaction].

1 22. (Amended) The method of claim 21, further comprising the acts of:
2 defining a sequence of desired bus transactions; and
3 assembling the sequence of desired bus transactions into [an object file
4 comprising] instruction words [representing predefined bus stimuli

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that, when applied to a bus, implement the sequence of bus transactions], wherein the sequence of bus transactions are executed when the instruction words are converted to signals and driven on the bus.

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23. (Amended) The method of claim 21, further comprising [the act of] providing predefined signals to the bus in response to signals received from the bus.

24. (Amended) The method of claim 21, further comprising [the act of] exchanging data with agents on the bus.

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29. (Amended) A system [to test a bus] comprising:
[at least one] an instruction memory to store a plurality of predefined bus stimuli [instruction] instructions, the predefined bus stimuli [instruction] instructions representing signals associated with a plurality of bus [transaction] transactions on [the] a bus;
at least one phase generator coupled between the bus and the instruction memory, the at least one phase generator to provide signals to the bus corresponding [in response] to the predefined bus stimuli [instruction] instructions.

30. (Amended) The system of claim 29, wherein the predefined bus stimuli [instruction] instructions also [represents] include the manner in which the signals are to be transmitted.

Please add the following new claims:

1 31. a method comprising:
2 generating a plurality of instructions words corresponding to a predefined
3 sequence of bus transactions;
4 storing the instructions words in a memory; and
5 executing the bus transactions by converting the plurality of instruction words
6 into signals and driving the signals onto the bus in the predefined
7 sequence.

1 32. The system of claim 1, further comprising:
2 an interface other than the bus coupled to the instruction memory, the interface for
3 connection with a device to receive a plurality of predefined bus stimuli
4 instructions.

1 33. The system of claim 1, wherein the plurality of predefined bus stimuli
2 instructions are configured as to drive a predefined ordered sequence of
3 bus transactions onto the bus.